Amendments to the Specification:

Please replace the paragraph bridging pages 1 and 2 (page 1, line 20 to page 2, line 4), with the following replacement paragraph:

It often happens that both the n-type transistor and the p-type transistor are integrated in a single chip as a large scale integrated (LSI) circuit. In this event, each transistor is formed on a silicon substance, such as a silicon substrate, a silicon film and the silicon substance usually has a surface with a (100) crystal plane orientation. Such silicon substance and such a surface with the ~~(110)~~ (100) crystal plane orientation may be referred to as a (100) silicon substance (or simply a ~~(110)~~ (100) silicon) and a (100) surface, respectively.

Please replace the second full paragraph on page 5, lines 12-17, with the following replacement paragraph:

Herein, a mobility of a carrier in a field effect transistor is one of factors showing the drivability of the transistor. As well known in the art, a hole is the carrier in the p-type field effect transistor while an electron is the carrier in the ~~p-type~~ n-type transistor. In general, it is necessary to raise up a mobility of a carrier by lessening a surface roughness of the element region so as to improve the drivability of the field effect transistor.

Please replace the fourth full paragraph on page 8, lines 17-20, with the following replacement paragraph:

The prescribed arithmetical mean deviation of surface of the silicon surface roughness Ra may ~~not~~ be not greater than 0.11 nm. Preferably, the prescribed arithmetical mean deviation of surface Ra is not greater than 0.07 nm.

Please replace the tenth full paragraph on page 16, lines 22-24, with the following replacement paragraph:

Fig. 16 shows a graphical representation for use in describing a relationship between repeat times of the first and the second processes and the ~~thickness~~ flatness;